Fbb CMOS Tapered Buffer With Optimal V_{th} Selection

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Abstract: This paper represents fixed body biased CMOS Tapered Buffer which is designed to minimize the PDP (Power Delay Product) of the circuit. CMOS Tapered Buffers are often used for driving large capacitive load at high speed. Since there are tradeoffs between performance parameters of Buffer for minimizing its PDP value and due to technology constraints on the threshold voltage of MOS; one can vary the Vth up to certain limit while keeping the V_{DD} constant. The proposed work is helpful in designing power efficient CMOS Tapered Buffer. This is found that in proposed Buffer when Vth value for the first stage of inverter is taken between the range of ($0.2V_{DD}$ - $0.4 V_{DD}$), its performance gets improved in terms of power dissipation. This analysis is verified by simulating the 2-stage Tapered buffer using standard 180nm CMOS technology in Cadence environment. Analysis performed on the schematic shows that FBB (Fixed Body Bias) Tapered Buffer reduces the average power dissipation across capacitive load by 77 % and static power has been reduced to 18.3% at very less penalty in delay. Hence the proposed approach is suitable in the design of low power buffer for increasing the current capability of logic gate at optimal speed.

Keywords: Tapering factor, CMOS inverter, PDP, RBB, Average power, Threshold voltage

I. INTRODUCTION

A CMOS Tapered buffer is used to increase the driving ability of the logic circuitry whenever it is connected with large capacitive load. These are often used between logic gate and large capacitive load to increase its drain current strength. With advances in the VLSI technology, the use of inverting and

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non – inverting buffers is used to drive large fan out by logic gate so that they can deliver large current for fast response. These circuits are required which can drive the load at high speed while not degrading the performance of previous stages in the chain of inverters [1]. It was observed that after a certain length of devices, the logic levels starts degrading. The high level starts reducing from that of V_{DD} value. Such degradation causes noisy output and many errors. Therefore the signal needs boosting. This boosting is provided by the buffer. Figure 1 shows the schematic of N-stages Tapered Buffer driving capacitive load.
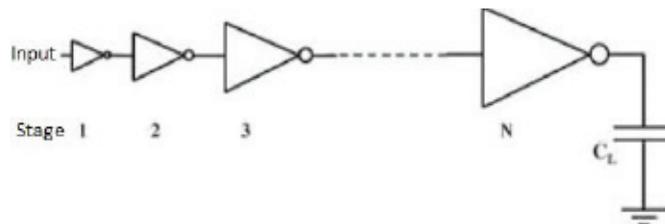
Figure 1: N-stage CMOS Tapered Buffer

High performance and low power dissipation in VLSI design is the attractive feature in latest portable systems. Increasing number of stages in Buffer chain to strengthen the input signal could increase its power dissipation. Thus less power dissipation in the buffer circuit demands a decrease in both V_{DD} and Vth to sustain propagation delay, but decrease in Vth increases leakage power and short circuit power exponentially. Similarly reducing C_L and increasing W/L ratio of the transistor for minimizing delay may increase self loading and output capacitance [2]. So this allows trade-off between different parameters for reducing both power and delay for the CMOS inverter circuit.

Since active area of recent research is to reduce power utilization of the CMOS transistors, hence power efficient buffers are always essential. Static power remains constant in digital designs, but sub-threshold leakage power tends to increase with scaling of the technology. This power can be reduced with the increase in threshold voltage or reducing the value of operating voltage V_{DD}. But the effect of increasing or decreasing threshold voltage while keeping V_{DD} fixed has very small impact on the delay of the circuit [16]. The proposed strategy can be helpful to vary threshold voltage of CMOS transistors. Because varying the threshold voltage of MOSFET by varying the width or tapering factor of the transistor could affect the PDP of the circuit due to large area utilization [7, 8]. So Buffer designing demands an approach which could resolve the issues related to PDP. The optimal values of primary factors for implementing Buffer design also play an important role. And expressions related to Tapering

factor and optimum number of stages used in the implementation of Buffer is mentioned in [6] and are given below using equation (1).

$$N_D = \frac{\ln(C_L/C_g)}{\ln(F)} \text{ where } F = \left(\frac{C_L}{C_g}\right)^{\frac{1}{N_D}} \quad (1)$$

Here Cg and C_L are gate capacitance and load capacitance and F is Tapering factor

Using these parameters, the value of propagation delay of Buffer can be calculated using equation (2) as given in [7].

$$T_{delay} = N \text{ VDD} \frac{C_D + FC_g}{I_{DO}} \left[\left(1.125 \frac{V_{DO}}{0.8V_{DO}} \ln\left(\frac{10V_{DO}}{eV_{DO}}\right)\right)\left(\frac{1}{2} - \frac{1-vt}{1+\bullet}\right) + \frac{1}{2}\right] \quad (2)$$

Where V_{DD} is applied D.C voltage to buffer circuit its operating value is based on technology node, V_{DO} and I_{DO} are the saturation drain voltage and saturation drain current at $V_{GS} = V_{DD}$, is velocity saturation index and = Vth / V_{DD}.

The total power dissipation in a CMOS tapered buffer can be calculated using equation (3) according to [4, 5] and its components are expressed separately. The expressions for three types of power are given in the equations (4), (5) and (6) that are taken from [1].

$$P_T = P_{dyn} + P_{S.C} + P_{static} \quad (3)$$

$$P_{dyn} = C_L * V^2_{DD} * f \quad (4)$$

Where C_L is capacitive load, V_{DD} is V_{DC} applied and f is the frequency of operation

$$P_{static} = I_{static (leakage)} * V_{DD} \quad (5)$$

Where $I_{static (leakage)}$ is the leakage current of MOS in idle state

$$P_{avg(short-circuit)} = [k f (V_{DD} - Vthn - |Vthp|)^3] \quad (6)$$

Where Vthn and Vthp are the threshold voltages of NMOS and PMOS and k is power constant

Short circuit power dissipation is assumed to be negligible in many designs, because NMOS and PMOS in the CMOS inverter remain ON for very short duration of time. It depends on the values of rise and fall time of applied signal thus we can control this power by controlling Vth and rise/fall time of input pulse.

Equation (4) shows that the dynamic power is the function of frequency, applied voltage and value of capacitive load. Since large value of capacitive

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loads are often used with Tapered Buffer and values of 'f' and V_{DD} are decided according to the technology node used, so another alternate is required to reduce dynamic power in Tapered buffers. Our main emphasis is to reduce the static power of circuit in Tapered Buffers.

The static power or leakage power is the power which is dissipated by Buffer in OFF state and it is the function of sub threshold leakage current and V_{DD} applied to the drain terminal of MOS. The main components of leakage current are sub threshold leakage (I_{Subth}), gate induced drain leakage (IGIDL), gate tunneling leakage (IGATE), and bang-to-band tunneling (IBTBT) and in on-state, gate tunneling leakage (IGATE) is the main component. The sub threshold leakage is a weak inversion conduction current that flows from source to the drain of the CMOS transistor when $Vgs < Vth$. It increases exponentially due to reduced threshold voltage, and is a main leakage component in high forward body bias [10]. But if the value of Vth increases with RBB the sub threshold power gets reduced because it is the function of sub threshold leakage current in the idle state.

Since reduction in Vth causes transistor sub threshold leakage current (Is*ub*) to increase exponentially and furthermore, other components of leakage current, e.g., the gate leakage and reverse-biased junction Band To Band Tunneling (BTBT) become important as we scale fabrication technology to 45 nm and downwards. In addition to the increasing dominance of leakage power, the sub threshold leakage and the gate-oxide tunneling increase extremely rapidly (exponentially) with technology scaling, and dwarf dynamic power [9]. Hence, RBB is a method which is employed in the proposed work to have variation in threshold voltage. If we adopt a strategy to adjust the transistors sizing using optimal values of primary factors such that its delay could be optimized then we can take the benefit of power minimization using reverse body biasing in Tapered buffers.

II. CMOS TAPERED BUFFER DESIGNING PARAMETERS

The primary designing parameters of tapered Buffer are number of stages of CMOS inverters and increasing width defining tapering factor. The optimal values of these factors can be calculated or derived using equation (1) for optimal values of result parameters of Buffer. And conventionally number of stages needs to be varied for changing the threshold voltage of the circuit. The increase in number of stages could increase the power dissipation or its cost function. Another approach is the use of FBB for varying Vth in Buffers.

The threshold voltage refers to the switching voltage of the inverter. This can be defined as the gate voltage at which a MOS transistor begins to conduct.

The threshold voltage can be given by equation (7) as mentioned in [13]

$$V_{th} = V_{THO} + \bullet(\sqrt{|-2 \bullet F + V_{SB}|} - \sqrt{|-2 \bullet F|}) \qquad (7)$$

Where V_{TH0} is the threshold voltage at V_{SB} =0V and it can be expressed as

$$V_{THO} \bullet \quad + 2 \bullet F + \frac{Q_{dep}}{C_{ox}} \qquad (8)$$

Here γ is body effect coefficient (which is Positive for NMOS and Negative for PMOS), ϕF is the Fermi potential with respect to mid gap in the substrate (which is Negative for NMOS and Positive for PMOS). This equation states the effect on threshold voltage due to source to body bias voltage i.e. by adjusting the V_{SB} (Voltage between source and body terminals of MOS) we can have control over the threshold voltage of the device. Otherwise Generally V_{SB} is taken as zero volts for all circuits.

The schematic symbol of 2-stage conventional Tapered Buffer is shown in Figure 2 where it is shown that the first CMOS inverter is minimum sized inverter and the size of second CMOS inverter is based on the optimal value of tapering factor. This Buffer is driving capacitive load. Other designing parameters of Buffer are dependent on the technology node used for implementation like value of V_{DD}, Vpulse and frequency of operation. For 180nm technology, V_{DD} is taken as 1.8 V, Vpulse = 0 V to 1.8 V and f = 50 MHz for design implementation.

Conventional method of varying Vth in CMOS Tapered Buffers is firstly varying the number of stages of inverters for Nopt and then calculating V_{th} analytically using equation (9). Using the expression of optimum
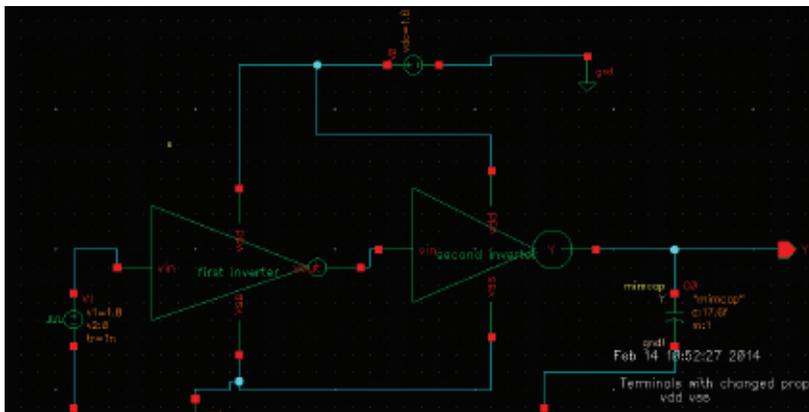
Figure 2: Schematic symbol of 2-stage Conventional CMOS Tapered buffer

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value of threshold voltage for arbitrary number of stages 'N', PDP can be derived analytically using expression (PDP = Propagation delay * Power Dissipation).

$$V_{th_{opt}} = \left(0.35 - 0.07\frac{N - N_{opt} - 1}{N_D - N_{opt}}\right)\left(1 + \ln\left(\frac{k_a}{2k_b}\right)\right) \qquad (9)$$

Where is the power dissipation weighing factor exponent and is the propagation delay weighing factor exponent and the expression for Nopt is represented in equation (10). The value of Nopt is used to calculate   for the design.

$$N_{opt} = [N_D\{1 - e^{-0.7(ka/kb)}\} - 1] \qquad (10)$$

Where N_D represents the number of stages in the buffer chain to achieve minimum delay irrespective of its power dissipation

It can be seen that for a particular value of Nopt, $V_{th_{opt}}$ yields minimum of Cost Function in the conventional Buffers. Since the value of Fopt is dependent on Nopt, thus large W/L ratio of cascading CMOS inverter stages could increase the power dissipation of the conventional Buffers.

The basic idea of the modified circuit is to observe the threshold voltage value for NM0 at which average power dissipation across load capacitor is least for the appropriate Reverse Bias voltage V_{SB}. The particular value of V_{th} for first inverter was explored and tested using simulation in Virtuoso at which there is least average power dissipation across C_L (dynamic power). This particular value of Vth (Vth = 0.3 V_{DD}) for NM0 also provides reduced static power for the low power Tapered buffer design. The body bias voltage is applied to NMOS using extra V_{DD} layer or it can be applied using body bias generators that are mostly used with recent logic circuits.

Table1 shows the results of 2-stage conventional and proposed Buffer for delay, Vth values and power dissipation of NMOS for particular value of C_L.

Table 1: Effect of variation of Vth on the output parameters of Conventional and Proposed Buffer

Type of Tapered Buffer	C_L	N	F	Propagation delay	Power Dissipation (P_d) across C_L	V^{th} of NM0
2-stage Conventional	17.6fF	Nd = 2	5.067	178.1 ps	-12.66 nW	.527 V
2-stage Proposed	17.6 fF	Nd = 2	5.067	186.2 ps	-2.96 nw	.554 V

The motivation of this research work is to develop such a low power speed optimized circuit that works efficiently at circuit level at particular value of threshold voltage of the circuit.

III. PROPOSED METHODOLOGY

Low power high speed CMOS Tapered Buffer are always essential for current amplifying ability, but it has been observed that they now a major source of power dissipation because of their number of stages. The conventional method of varying Vth was to vary the number of stages in the Buffer chain (like Nopt) which could provide low power dissipation at large expense of delay. And there is trade-off between various parameters on which delay and power consumption of Buffer are based. Thus there is a need for a new approach that while reducing the delay, also consumes less power.

The reverse body bias (RBB) is the type of Fixed Body Biasing scheme which is used to decrease the leakage current by increasing the threshold voltage Vth of the circuit [12]. Thus one can reduce the value of Vth while keeping the V_{DD} constant. The reverse body bias technique is helpful to reduce leakage current of the idle portions of the logic circuits and short circuit power in the proposed buffer chain. Table 2 shows the set of values used for designing conventional and proposed buffer for simulation using Cadence tool.

Table 2: Design Parameters of Conventional and RBB Tapered Buffer

Value of $V_{D.C}$ Source	Value of Input V_{PULSE} Source	Frequency of Operation	Rise and Fall time of Input Pulse	Time period of Input Pulse
1.8 V	Switching between 1.8 V to 0 V	50 MHz	1 ns	20 ns

It has been proved that the problem of large static power dissipation can be minimized by varying the threshold voltage using Fixed Body Biasing or Adaptive body biasing [18]. Since switching power could be reduced by lowering V_{DD} or using low values of frequency of operation and C_L, which are not practically possible solutions for reducing dynamic power of Tapered buffer. Thus, RBB scheme can resolve the power issues in Digital logic Buffers. For reverse bias, the body terminal of NMOS used in first stage of the buffer chain is connected to the negative potential of the bias dc source as shown in the Figure 3. In standby mode or idle mode of operation, RBB is very helpful for minimizing leakage power.

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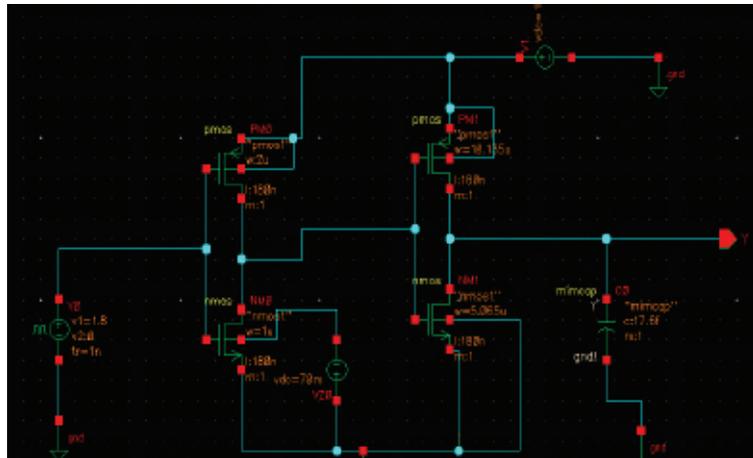
Figure 3: Schematic of 2-stage RBB Tapered Buffer

Body biasing of NMOS has been implemented by applying low voltage between substrate and source terminals of NM0. Body biasing can vary Vth of a MOS without varying the value of V_{DD}. Forward body bias scales down the threshold voltage and reverse body bias increases the threshold voltage. Thus by applying RBB we can reduce leakage current, static power and the average power of the design at vary small penalty in delay.

IV. OPTIMIZATION OF PERFORMANCE PARAMETERS

Low power has emerged as a principle theme in today's world of VLSI industries. Power dissipation has become an important consideration for designing buffer because these circuits are not only amplifies the signal but also drive the large capacitive loads with high driving speed. For many designs optimization power is important for extended battery life of portable systems. The CMOS Tapered Buffer with optimal value of its primary factors can be an effective strategy for designing optimized Buffer. The optimization of total power dissipation can be achieved by minimizing any of its power components as mentioned in Equation 3.

Since the static power consumption of a CMOS inverter is dependent on the static current as well as on the leakage current. AND there is no static current in CMOS when $V_{in} < V_{thn}$, but the leakage current which is influenced by width of MOSFETs, supply voltage and the threshold voltages can be determined by OFF MOSFET [15]. The significance of implementing proposed technology in the conventional circuit design is to reduce leakage power dissipation and

dynamic power across the capacitive load with minimal increase in propagation delay.

For reducing short circuit current the Fast rise/fall times on input V_{PULSE} signal are set to small values as discussed in [4] and for reduced input capacitance small size gate is used because by Inserting small transistors (leakage proportional to width) leakage power can be controlled. The 2-stage schematic of tapered Buffer is used for performing different types of analysis using ADE L window for the results of performance parameters. When the optimum body bias is detected, the body voltage adjustments are stopped to avoid excessive reverse body bias [11]. However, if the RBB is too high, the leakage current may inadvertently increase. The optimum RBB point can vary with process and temperature variations. Hence a scheme such as ours that can dynamically find the optimum RBB point can help greatly. Also the scheme itself does not consume very high power and it has a very modest silicon area requirement.

An increase in the threshold voltage of the device keeps the Vgs of the NMOS transistor safely below the Vthn. This is the case for logic zero input. For the logic one input increase in the threshold voltage of the device keeps the Vgs of the PMOS transistor safely below the Vthp [18]. This is the advantage of using RBB which can help to vary the switching voltage or threshold voltage of CMOS inverter. Figure 4 shows the effect of RBB on delay and power of the proposed Buffer. It can be seen that delay value is decreasing with decrease in RBB voltage values, and average power of C_L is decreasing with the decrease in reverse body bias voltage upto certain limit then it tends to increase.
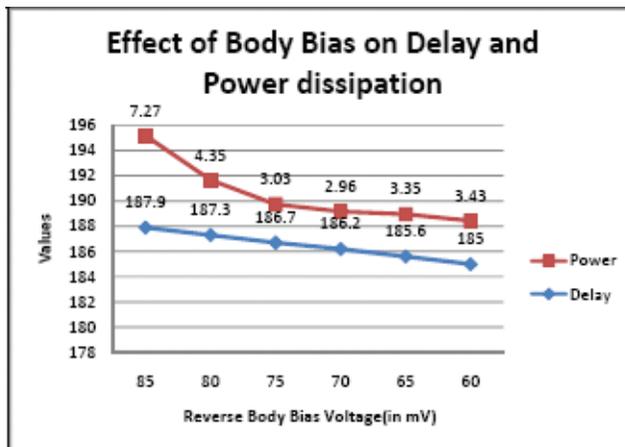
Figure 4: Graph showing the effect of RBB on delay and Power of Proposed Tapered buffer

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The slight increase in the value of reverse body bias tends to increase threshold voltage for MOS. The effect of increasing threshold voltage for NMOS of the first stage in Buffer chain helps to minimize its power dissipation. Thus it has been proved that average power dissipation of Buffer gets reduced for a particular value of Vth.

V. EXPERIMENTAL RESULTS AND DISCUSSIONS

The schematics of 2-stage conventional and proposed Buffers are designed using Virtuoso Schematic Editor of version 6.1.5. The proposed optimal body bias technique using 180nm technology has been simulated in Virtuoso window using Cadence tool. The results of performance parameters of Buffer were calculated using calculator window after obtaining its input-output waveforms. The print values of result parameters are taken by clicking on MOS in schematic window.

Table 3 shows the simulation results of Conventional Buffer and RBB Buffer for 2-stage Tapered Buffer after its circuit analysis.

Table 3: Comparison of results for different types of power for RBB and Conventional Buffer

Fixed Body Biasing voltage for NM0	Static Power (in pW)	Average V_{dc} source power (in µW)	Average Power dissipation across C_L (in nW)	% decrease in Static Power dissipation	% decrease in Average power dissipation across C_L
Conventional	68.62	18.97	12.66	Taken for comparison	Taken for comparison
60 mV	57.41	18.86	3.42	16.3%	73%
70 mV	56.09	18.82	2.96	18.3%	77%
80 mV	54.9	18.80	4.35	20 %	66%

It is shown in the result Table 3 that when the value of FBB is 70mV the proposed buffer provides maximum % decrease in Average power dissipation across C_L. The RBB of 70mV for first stage refers to (Vth = 0.3 times V_{DD}) for that particular stage.

After that d.c and transient analysis was performed using ADE L window to get d.c response of proposed Buffer which is shown in Figure 5. The transient analysis was required to get output logic waveform for pulse input and output waveform is required for calculating propagation delay of the Buffer. D.C
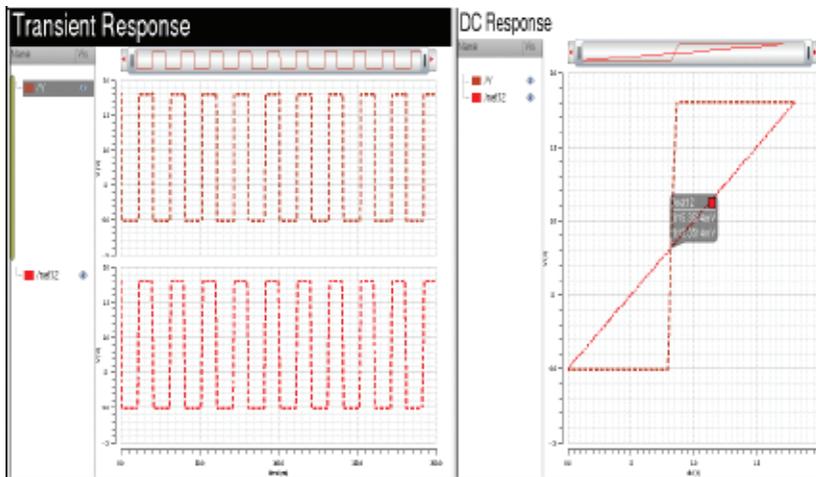
Figure 5: Input Output waveforms of 2-stage RBB Tapered Buffer

analysis was performed to determine the switching voltage of the circuit. The intersection point of input output waveform gives the value of switching voltage of the inverter which is around half of V_{DD} value used (shown value is 815.35 mV).

The tran-tran response is the third type of analog design analysis which was performed on the schematic to get to know the value of its static power (leakage power) consumption. In Figure 6 it has been shown that the value of static power can be taken by placing the cursor of mouse on the: pwr curve. The value of propagation delay and average power dissipation of proposed Buffer is calculated using calculator window in Virtuoso. The values of result parameter of 2-stage Tapered Buffer are then compared with the conventional 2-stage Tapered Buffer.

VI. CONCLUSION AND FUTURE WORK

It can be concluded that the FBB doesn't add any overhead in performance of the design except extra V_{DD} layer. The proposed work not only improves the performance parameters of Tapered Buffer but also provides the optimal value of Vth for which Buffer dissipates least Average power. The proposed Tapered buffer design has reduced the average power dissipation across C_L by 77% as well as static power reduction by 18.3% at very less penalty in delay. This work can be extended with the use of mixed body biasing (FBB and RBB) in processor designs and achieve decrease in the leakage powers in Low Power

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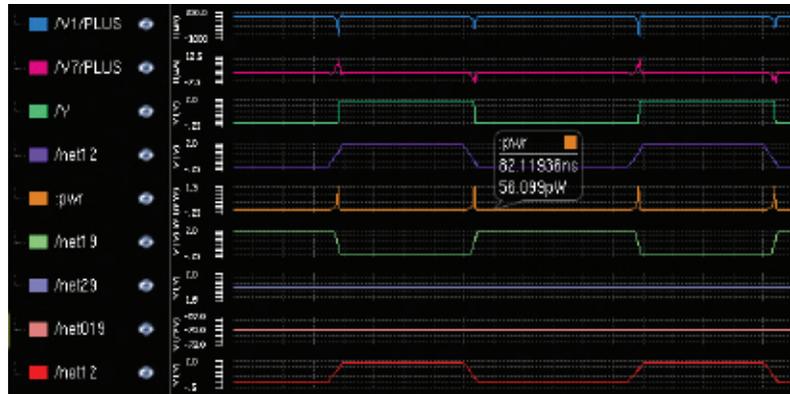
Figure 6: Tran-Tran response of 2-stage RBB Tapered Buffer

Mode and decrease in the critical path delays in Active Mode of Operations. The proposed approach can be helpful in dual Vdd circuit or in multiple supply system, where a high-voltage supply is used for high-performance circuits and a low-voltage supply is used for low-performance circuits. Still there is lot of research work required in this domain so that instead of using of extra V_{DD} layer for the body biasing of NMOS, Adaptive body bias generators could be used for providing that particular value of body bias voltage for the first CMOS inverter.

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