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Design of RF Low Noise Amplifier at 2GHz in 0.18µm Technology

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Abstract: A 2GHz Low Noise Amplifier (LNA) has been implemented in Cadence Spectre RF tool on UMC 0.18µm technology and is designed using a modified Cascode topology to work under reduced power supply. The input and output matching network is matched to 50Ω. After simulation it is found that at resonance frequency of 2GHz, the forward gain is 18.22dB and reverse isolation is -40.86dB.

Keywords: RF circuit design, Low Noise Amplifier, 0.18µm technology.

1. INTRODUCTION

The semiconductor industry has transformed the complete system on a single chip with the increase in growth of wireless and telecom applications. Wireless systems comprise of a front-end and a back-end section. The front-end section processes analog signals in the high radio frequency (RF) range from 100 KHz to 100 GHz while the back-end section processes analog and digital signals in the baseband low frequency range below 1 GHz.

RF circuits must be able to process analog signals available at high frequencies. The signal must be treated as analog even if it is digital modulation. Design of such circuits are having some trade-offs that can be summarized in the "RF design hexagon" [1] shown in Figure 1, where almost any two of six parameters trade with each other to some extent.

The radio frequency signal received at the antenna is weak. Therefore, an amplifier with a high gain and good noise performance is needed to amplify this signal. Such an amplifier is referred to as a Low Noise Amplifier (LNA) and forms an essential component of any RF integrated circuit receiver. The

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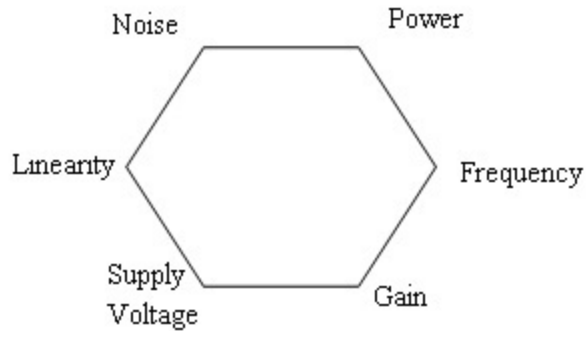


Figure 1: RF design hexagon.

total noise performance of the receiver depends on the Gain and Noise Figure of the LNA, as calculated by the Friss equation [2] used in antenna theory.

$$F_{cascade} = F_{stage1} + \frac{F_{stage2\text{-}1}}{Gain_{stage1}} + \frac{F_{stage2\text{-}1}}{Gain_{stage1} \times Gain_{stage2}} + \cdots \quad (1)$$

$$NF = 10Log_{10}(F) \quad (2)$$

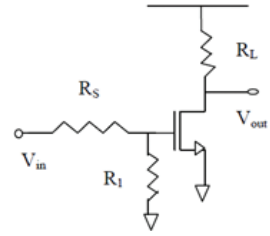
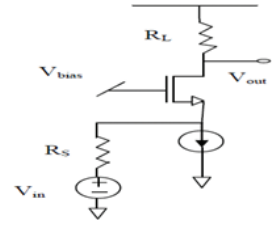
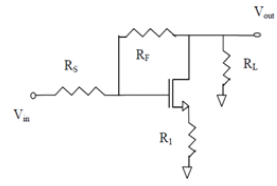
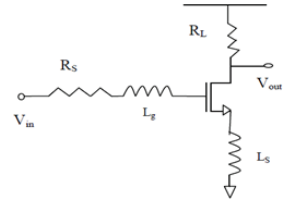
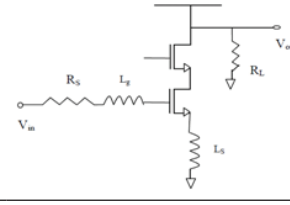
In the above equations, Gain stands for the power gain of the particular block and stage1, stage2, stage3 are the cascade blocks of the receiver from the antenna to the demodulator. Since the LNA forms the first major stage of the receiver therefore, as evident from equation (1), its gain and noise performance contributes significantly towards the total noise performance of the receiver. The general topology of the LNA can be broken down into the three stages: Input Matching Network, the Amplifier and the Output Matching Network. The performance of these blocks is characterized by the S-parameters S11, S12, S21 and S22.

2. LOW NOISE AMPLIFIER

LNA is the first stage in the receiver design and is used to boost up the strength of the weak information signal of the desired frequency. The information signal suffers due to various types of noise which results in very small signal to noise ratio. Since, the operating frequency of LNA is in RF frequency band, the circuit should be as simple as possible, especially for the RF path. Otherwise, the circuit noise becomes too high. Moreover, if the circuit is too complicated, the parasitic effects may distort the amplified signal. Hence, there are several fundamental

LNA topologies for single ended narrow band low power low voltage design, such as resistive termination common source, common gate, shunt series. The advantages and disadvantages of different kinds of LNA topologies are shown in Table 1.

Table 1: Advantages and disadvantages of LNA topologies.

Type	Advantages	Disadvantages	Topologies
Resistive termination common source [1][3]	Broad band amplifier	Adding the noise from the resistor	
Common gate [1][3]	The input impendence is equal to $1/g_m$. It is practical to get 50 Ω.	The impedance varies with the bias current	
Shunt series feedback common source [1][3]	Broad band amplifier	Adding the noise from resistor	
Inductive degeneration common source [1][3]	The source and gate inductors make the input impendence 50 Ω. Not adding noise from the input	The inductor is off chip at low frequency and low isolation	
Cascode inductor source degeneration [1][3]	Isolation of input and output is good, higher gain, lower noise figure.	The inductor is off chip at low frequency.	

Out of the several topologies for narrow band single ended LNA design, an appropriate topology should be selected for low power and low voltage optimized LNA design.

3. CIRCUIT DESCRIPTION

The complete schematic of single ended LNA employing inductive source degeneration (inductor L_S connected to the source of transistor M_1) is shown in Figure 2.The advantage of this method is that the input impedance (real part) can be controlled through the choice of inductance. Cascoding transistor M_2 is used as a voltage buffer to reduce the interaction of the tuned output with the tuned input. Coupling capacitance C_0 is used to couple the RF input to the gate of the amplifier. Transistor M_3 is the biasing transistor and forms a current mirror with transistor M_1. To minimize the power overhead of the bias circuit the width of M_3 is kept a small fraction of the width of M_1. To maximize the output power transfer and gain at resonance frequency output inductor, L_d resonates with output load. The width of the Cascoded transistor must be sized to trade-off common source gain reduction and increase of parasitic source capacitance of M_2 (both are consequence of a wider M_2). Cascode transistor helps to reduce S_{21} and reduce C_{gd1} Miller effect. R_{bias} is large enough so that its equivalent current noise is small enough to be ignored. The resonant frequency is set using Lg.

The design procedure followed for the design of single-ended LNA is Power optimization based [3][4].

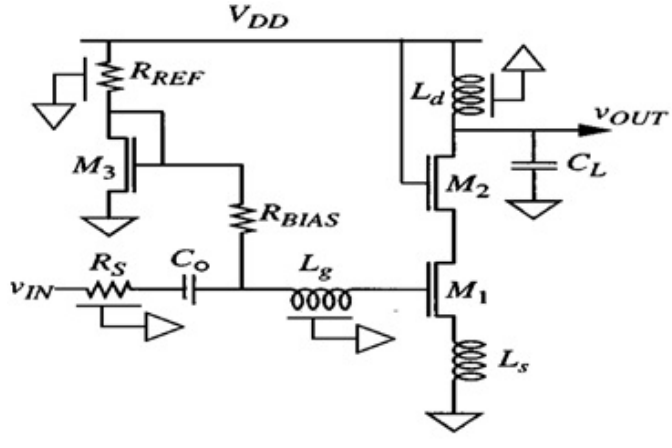


Figure 2: Single Ended Low Noise Amplifier.

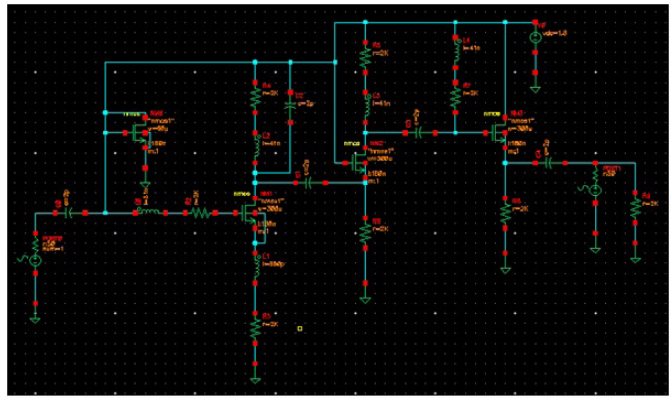


Figure 3: Schematic of the Single Ended Low Noise Amplifier.

1. Input impedance: The input impedance of the inductively degenerated Cascode LNA is given by [3]

$$Z_{in} = S(L_g + L_s) + 1/(S_{Cgs}) + g_{m3} * L_s / C_{gs} \tag{3}$$

$$\omega_T = g_{m3} / C_{gs} \tag{4}$$

$$So, Z_{in} = S(L_g + L_s) + 1/(S_{Cgs}) + \omega_T * L_s \tag{5}$$

At resonance, impedance is purely real resistive and proportional to

$$Z_{in} = \omega_T * L_s = g_{m3} * L_s / C_{gs} = 50\Omega \tag{6}$$

2. Find the optimum device width: The optimal value of Q in case of power optimization technique is[3]

$$Q_{L,opt,PD} = |C| \sqrt{\frac{5\gamma}{\partial}} \left[1 + \sqrt{1 + \frac{3}{|C|^2} \left(1 + \frac{\partial}{5\gamma} \right)} \right] \tag{7}$$

The equation for the device width is

$$W_{M1,opt,PD} = \frac{3}{2\omega_o C_{ox} L R_s Q_{L,opt,PD}} \tag{8}$$

3. Find (Gate-Source capacitance):We know that

$$C_{gs}total = \frac{2}{3} C_{ox} * W * L + C_{ox} * W * L_D \tag{9}$$

4. Find the device transconductance ()

$$g_{M1} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_{M1} I_{DM1}} \tag{10}$$

5. Find the transistor unity gain frequency (ω_T)

$$\omega_T = g_{M1} / C_{gs1} \tag{11}$$

6. Expected noise figure4]

$$F_{min,PD} = 1 + 2.4\frac{Y}{\alpha}\left(\frac{\omega_o}{\omega_T}\right) \geq 1 + 1.62\left(\frac{\omega_o}{\omega_T}\right) \tag{12}$$

7. Starting value of Degeneration Inductor L_S: The value of this inductor is fairly arbitrary but is ultimately limited on the maximum size of inductance allowed by the technology, which is typically about 10nH.

$$Z_{in} = \omega_T * L_S \tag{13}$$

$$L_S = Z_{in} / \omega_T \tag{14}$$

8. Evaluation of : We know,

$$L_g = \frac{1}{C_{gs}\omega_o^2} - L_S \tag{15}$$

9. Evaluation of L_d:

$$L_d = \frac{1}{CL\omega_o^2} \tag{16}$$

10. Width of transistors: Size of M_3 is chosen to minimize power consumption. So M_3 = 60 μm. size of M_1= M_2, So that they can have shared drain area. It can reduce the impedance looking into gate and drain of M_1 degrading the input match and noise performance, so both transistors sizes are to made equal. Transistor M_2 is used to reduce the miller effect.
11. Value of bias resistor: R_{bias} must be large enough so that its equivalent current noise can be neglected. R_{bias}= 2KΩ
12. Calculation of power dissipation (P_d):We know,

$$P_d = V_{dd} * I_d \tag{17}$$

4. SIMULATION RESULTS

The various simulation iterations are performed on the proposed LNA circuit to meet design requirements. After the simulation of the single-ended LNA at 2GHz frequency obtained results in terms of S parameters are shown in the below figures. The input return loss value or input reflection coefficient can be expressed in terms of S_{11} is −12.21dB as shown in Fig. 4. Similarly (transmission) reverse gain S_{12} parameter is-40.86 dB as shown in Fig. 5 and

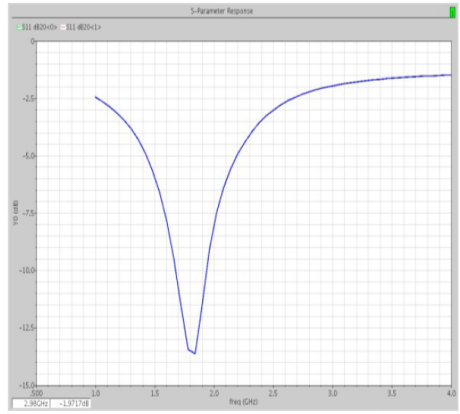


Figure 4: Plot for S_{11} parameter of single ended LNA.

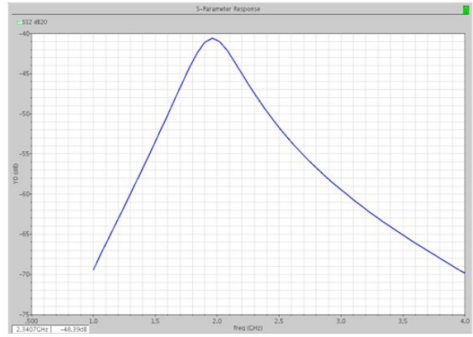


Figure 5: Plot for S_{12} parameter of single ended LNA.

Fig. 6 show the S_{21} parameter is 18.22dB i.e. the power gain at 2GHz frequency. Fig. 7 show the S_{22} parameter is −12.21 dB.

The simulation results of single-ended LNA achieved at the typical process are summarized in the Table 2.

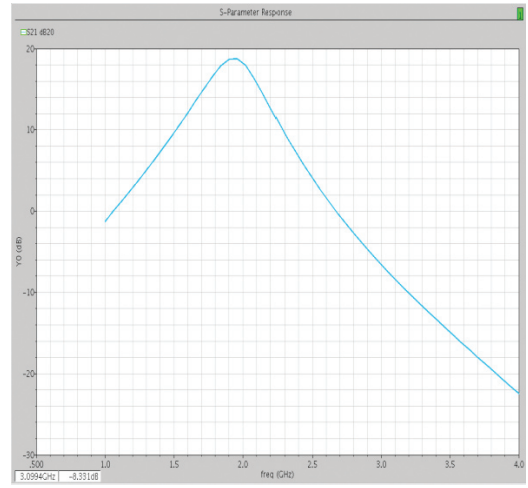


Figure 6: Plot for S_{21} parameter of single ended LNA.

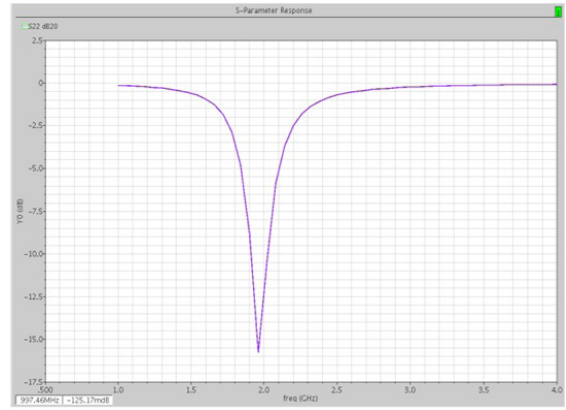


Figure 7: Plot for S_{22} parameter of single ended LNA.

Table 2: Simulation Results (S-Parameters).

Performance Parameter	Standard Value of LNA	Experimental/Simulation Value	Unit
Power Gain (S_{21})	10-20	18.22	dB
S_{22}	<-10	-12.21	dB
Return Loss (S_{11})	<-10	-8.032	dB
S_{12}	<-20	-40.86	dB

5. CONCLUSION

A low noise amplifier is designed and simulated using CADENCE SPECTRE tool in 0.18μm technology. It is found that the value of S_{11} parameter is -8.032 dB, S_{12} parameter is -40.86 dB, S_{21} parameter is 18.22 dB, S_{22} parameter is -12.21 dB.

REFERENCES

[1] Behzad Razavi, "RF MICROELECTRONICS", Second Edition, Prentice Hall Publications.

[2] Derek K. Shaeffer and Thomas H. Lee, "A 1.5V, 1.5 GHz CMOS Low Noise Amplifier", IEEE J. Solid-State circuits, Vol. 32, pp. 745-759, May 1997. http://dx.doi.org/10.1109/4.568846

[3] Hafez Foud, Khaled Sharaf, Essael-Diwany and Hadia El-Hennawy, "An RF CMOS modified Cascode LNA with Inductive Source Degeneration", In Proceedings of nineteenth National Radio Science Conference, pp. 450-457, March 2002. http://dx.doi.org/10.1109/NRSC.2002.1022654

[4] Jeonghoon Lee, Youngsik Kim, "A 1.8 Fully Differential CMOS Low Noise Amplifier with a special care for Mixer Input Stage", IEEE SIRF, pp. 178-181, 2006

[5] M. Sumanthi and S. Malarvizhi, "Performance Comparison of RF CMOS Low Noise Amplifiers in 0.18 μm technology scale", International Journal of VLSI design & Communication Systems, Vol. 2, No. 2, pp. June 2011.

[6] Matthew N. O. Sadiku, "Principles of Electromagnetics", Fourth Edition, Oxford University Press.

[7] Pranjal Rastogi, J. Karthik and Rajnish Sharma, "Design of an RF CMOS LNA using 0.25 micron technology", VDAT.

[8] Tajinder Manku, "Microwave CMOS – Devices and Circuits", IEEE Conference in Custom Integrated Circuits, pp. 59-66, 1998

[9] Thomas H. Lee and S. Simon Wong, "CMOS RF Integrated Circuits at 5GHz and Beyond", In Proceedings of IEEE, Vol. 88, No. 10, October 2000. http://dx.doi.org/10.1109/5.888995

[10] Trung-Kein Nguyen, Chung-Hwan Kim, Gook-JuIhm, Moon-Su Yang and Sang-Gug Lee, "CMOS Low-Noise Amplifier Design Optimization Techniques", IEEE Transactions On Microwave Theory And Techniques, Vol. 52, No. 5, pp. 1433-1441, May 2004. http://dx.doi.org/10.1109/TMTT.2004.827014

[11] W.R.Liou, C.A. Tsai, M.L. Yeh and G.E. Jan, "A 5.2 GHz low-voltage Low-Noise amplifier with 0.35μm CMOS technology", International Journal Of Electronics, Vol. 91, No. 9, pp. 551-561, September, 2004. http://dx.doi.org/10.1080/00207210412331319083